

Notice of References Cited	Application/Control No. 10/007,151		Applicant(s)/Patent Under Reexamination CORNABY ET AL.	
	Examiner William M. Treat		Art Unit 2183	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,629,236	09-2003	Aipperspach et al.	712/228
*	B	US-6,341,347	01-2002	Joy et al.	712/228
*	C	US-5,778,243	07-1998	Aipperspach et al.	712/11
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	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Chris Jesshope, "Implementing an Efficient Vector Instruction Set in a Chip Multi-Processor using Micro-Threaded Pipelines", Proceedings of the 6 th Australasian Computer Systems Architecture Conference, IEEE, 01/29/2001--01/30/2001, pp. 80-88.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.